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Field-Programmable Gate Array Implementation on Ethernet MAC for High Speed Secure Data Communication

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Abstract: Due to increasing network connectivity, low bandwidth, high power consumption, high cost, low performance, and information security are major issues in existing networks. To provide the high-speed connectivity and data security, FPGA (Field Programmable Gate Array) based solution plays an important role over a large network. This paper introduces the FPGA based implementation of Ethernet 1000BASE-X PCS/PMA and Tri-Mode Ethernet MAC cores for gigabit Ethernet communication at low cost, low power consumption and high performance over fiber optics as well as a copper medium. The implementation of RTL (Register Transfer Level) model is achieved to develop and integrate the mentioned cores using Verilog HDL (Hardware Description Language). The Verilog HDL code is simulated for customized Xilinx Spartan 3E FPGA Board using Xilinx ISE 14.7 Design Suite.

Keywords: Field Programmable Gate Array, Register Transfer Level, Hardware Description Language, Media Access Controller, Unshielded Twisted Pair

1. Introduction

The Gigabit Ethernet standard is the latest version of Ethernet standard defined by the IEEE 802.3-2008 standard. It also referred to as 1000BASE, GigE or 1GigE compatible with all existing Ethernet Systems. It provides 10 times faster transfer speed than Fast Ethernet (100BASE) with full and half-duplex [1, 2]. The most popular Gigabit Ethernet standards are 1000BASE-T and 1000BASE-X. The 1000BASE-T is the IEEE 802.3ab Gigabit Ethernet standard for GbE copper cables supporting CAT5e, CAT6, and CAT7 with maximum length to 300 meters. The 1000BASE-Xis the IEEE 802.3z Gigabit Ethernet standard for GbE over single-mode/multimode fiber optics. The OSI model is used to describe the behavior of network that consists of seven layers which are physical layer, data link layer, network layer, transport layer, session layer,

presentation layer, and application layer [3, 4]. Each layer of the OSI model has an important role in communication between nodes as described in Figure 1.

The physical layer (PHY) is partitioned in three sub-layers; Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and Physical Medium Dependent layer (PMD). The combination of the PCS, the PMA, and the PMD sub layers constitute the physical layers for the protocol [2].

Two main physical standards are specified as follows:

- **BASE-T:** PHY provides a link between the MAC and copper medium. This functionality is not offered within the TEMAC. However, external BASE-T PHY devices are readily available on the market. These can connect to the Ethernet MAC, using GMII.

- **BASE-X:** PHY provides a link between the MAC and fiber optic medium. The TEMAC is capable of supporting the 1 Gb/s BASE-X standard. The 1000BASE-X PCS and PMA sub-layers can be offered by connecting the TEMAC to the Ethernet1000BASE-X PCS/PMA or SGMII LogiCORE.

The PCS and PMA are also called the core of the physical layer. The PCS sublayer provides the functionality of 8b/10b encoding, decoding, and synchronization. At the transmitter side, the PCS deals with how to encode the information along with encoding rules during transmission. At the receiver side, the PCS deals with how to decode the information along with decoding rules during a reception [5]. The PMA sublayer provides the functionality of serializing and de-serialize of code group of information. The PMA sub-layer is used as SERDES to convert the data from parallel to serial during transmission at the transmitter side and from serial to parallel during a reception at the receiver side [1, 5]. Salem, et al. [6] implemented the 1000BASE-X PCS/PMA core for Gigabit Ethernet over fiber cable where the implementation of all building blocks including PCS, PMA, and GTX on Xilinx V6 ML605 Evaluation Board is achieved by using VHDL. In this paper, the implementation of 1000BASE-X PCS/PMA core with the use of GTX transceiver may provide high-performance serial connectivity. The proposed VHDL model was synthesized on Xilinx ISE Design Suite and simulated using Xilinx ISE 14.7 Simulator and Chipscope Analyzer for verification. The simulated results of the VHDL model were worked at 1.32 Gbps with reduced power consumption.

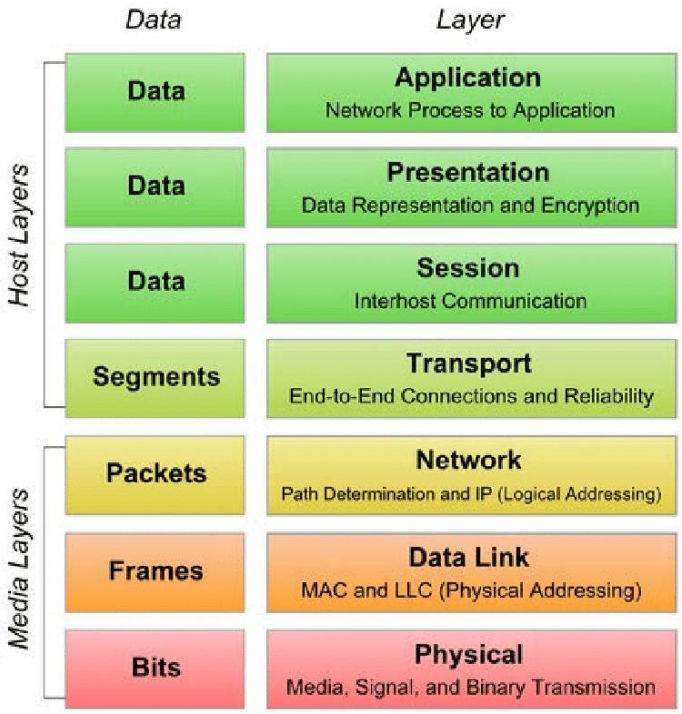

Figure 1. OSI Model

In this paper, 1000BASE-X PCS/PMA is implemented with TBI and Tri Mode Ethernet MAC cores using Verilog HDL for customized Sartan-3E (xc3s500e-4fg320) FPGA board with use of external serial connectivity for high performance embedded system. The Ethernet 1000BASE-X PCS/PMA or SGMII core use TBI interface to provide the functionality to

implement the 1000BASE-X PCS sub-layer with use of an external SerDes. It generates both 1000BASE-X PCS/PMA with TBI and Tri Mode Ethernet MAC cores separately through core generator and then integrate the 1000BASE-X PCS/PMA and Tri Mode Ethernet MAC after instantiating the all cores in a top wrapper to provide the gigabit Ethernet communication over fiber for one link. Again instantiate the 1000BASE-X PCS/PMA and Tri Mode Ethernet MAC to integrate them for providing gigabit Ethernet communication over other fibre link. These both fibre links provide high speed connectivity with external transceivers. Moreover all integrated cores are synthesized and generated the bit file for the design implementation. Then targeted board is configured by using JTAG. Design results are analyzed the on Xilinx ISE 14.7 simulator and ChipeScope Analyzer. In this proposed design, the 1000BASE-X PCS/PMA or SGMII core with TBI provide the high speed parallel interface to the external advance serial connectivity over the fiber optics. The simulated results show high performance at very low cost on customized Spartan 3e FPGA board.

This paper is arranged as follows: Section 2 presents the related work; Section 3 presents the proposed work in which internal structure functionality of 1000BASE-X PCS/PMA with TBI core, internal structure functionality of Tri Mode Ethernet MAC core and overall design architecture are described. Section 4 presents the simulation and results of proposed model and section 5 summarize the conclusion of paper.

2. Proposed Work

2.1 Ethernet 1000BASE-X PCS/PMA or SGMII core

Ethernet 1000BASE-X PCS/PMA or SGMII core with TBI provides the functionality to implement the 1000BASE-X PCS and PMA sub-layers with the use of external SerDes [6]. Alternatively, it can be used to provide a GMII. The core with TBI provides some of the PCS layer functionality such as 8B/10B encoding/decoding, and clock recovery [5]. The optional TBI is used to provide the parallel interface in place of Gigabit transceiver to external PMA SerDes. To replace some of the device-specific transceiver functionality, the addition logic blocks are required in the core as shown in Figure 2, it illustrates the remaining PCS sublayer functionality and the major functional blocks of the core.

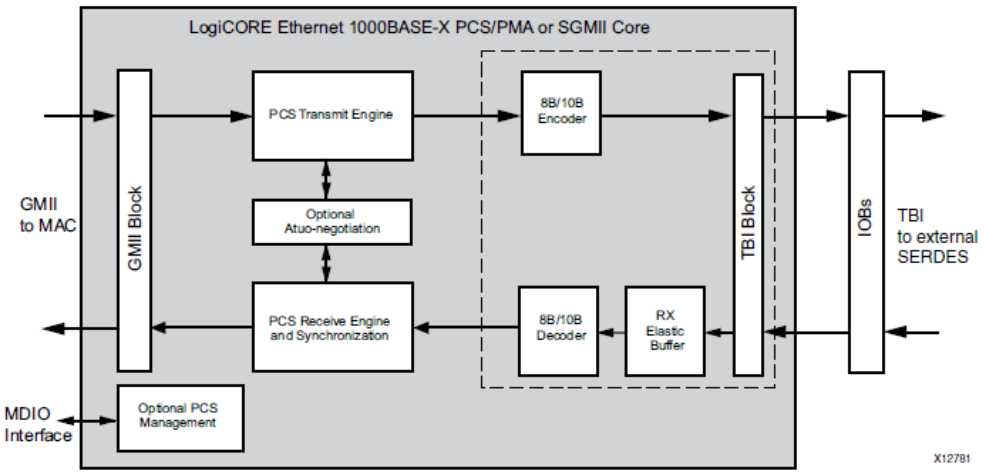

Figure 2. Function Block Diagram of 1000BASE-X PCS/PMA With TBI Interface [5]

The client-side GMII of the core can be used as an internal interface for connection to Ethernet tri-mode MAC or other custom logic. GMII provides independent 8-bit wide for transmitting and receiving data paths along with two additional one-bit signals for data validation and error. The GMII is operating at 125MHz, the PCS transmit engine converts the GMII data octets into a sequence of ordered sets and the PCS receive engine converts the sequence of ordered sets to GMII data octets. Auto-Negotiation block allows a device to advertise the supported modes of operation to a device at the remote end of a link segment (link partner) and to detect corresponding operational modes that the link partner might be advertising. Auto-Negotiation is controlled and monitored through the PCS Management registers. Configuration and status of the core, including access to and from the optional Auto-Negotiation function, is performed with the 1000BASE-X PCS Management registers as defined in IEEE 802.3-2008 clause 37. These registers are accessed through the serial Management Data Input/output Interface (MDIO), defined in IEEE 802.3-2008 clause 22.

An additional configuration interface is provided to program Control register (Register 0) and Auto-Negotiation advertisement (Register 4) independent of the MDIO interface. The PCS Management registers can be omitted from the core when the core is performing the 1000BASE-X standard. In this situation, configuration and status are made possible by using additional configuration vector and status signals. When the core is performing the SGMII standard, PCS Management registers become mandatory and information in the registers takes on a different interpretation. The transceiver interface block enables the core to connect to a device-specific transceiver. The Receiver Elastic Buffer provides the 10-bit parallel interface to receive the data from PMA sub-layer at TBI receiver clocks synchronously and to transmit onto the 8B/10B decoder at clock 125MHz. The Receiver Elastic Buffer is an asynchronous FIFO implemented in internal RAM. The Receiver Elastic buffer attempts to maintain a constant occupancy by the operation of inserting or removing idle sequences as necessary. That is why no corruption occurs in the frame of data.

The 1000BASE-X PCS/PMA core with TBI is designed to use with external SerDes [7]. Figure 3 illustrates the connections and transmitter logic required between the core and TBI block when TBI interface is used. The transmitter data signals are registered in the IOBs where the logic is used an IOB output DDR registers so that the clock signal produced the same delay as the data and control signals. The rising edge of inverted clock signal pma_tx_clk with respect to gtx_clk occurs in the center of the data valid to maximize and hold times across the interface. Figure 4 illustrates the uses of the pma_rx_clk0 clock as defined by the TBI specification. In this implementation, the DCM is used on the path of pma_rx_clk0 clock for phase-shifting to fine-tune the setup and hold times at the rx_code_group [9:0] IOB input flip flops. The output of DCM is inverted before routing it to the pma_rx_clk1 input of the core.

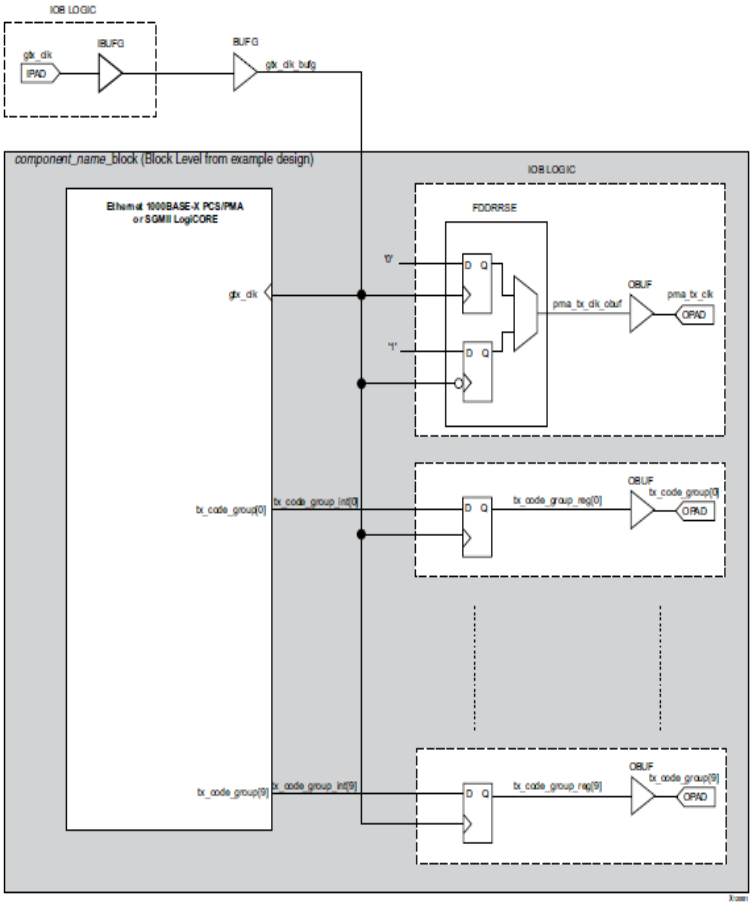

Figure 3. Ten Bit Interface Transmitter Logic [5]

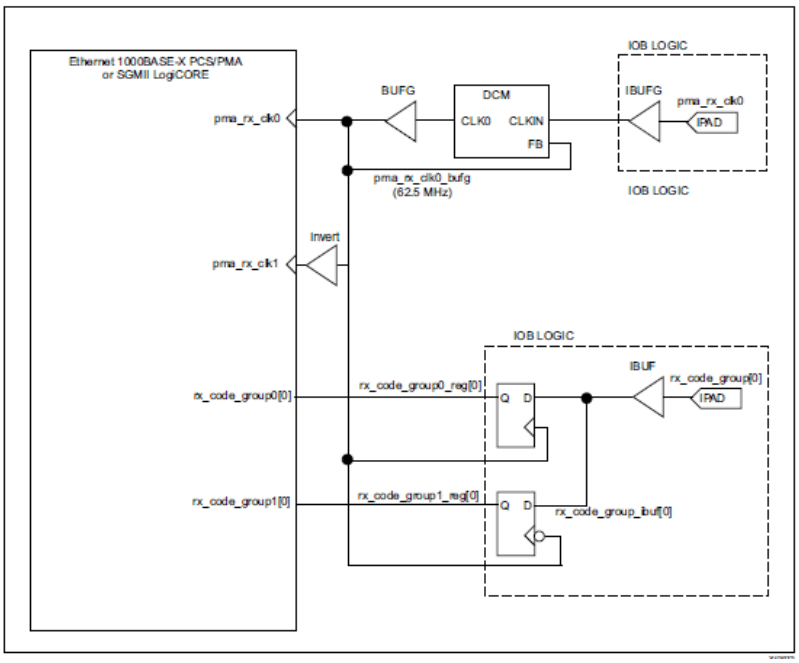

Figure 4. Ten Bit Interface Receiver Logic [5]

2.2 Tri mode Ethernet MAC

Tri-mode Ethernet MAC is defined in IEEE 802.3-2008, clauses 2, 3 and 4. It is responsible for the Ethernet framing protocols and error detection of frames. It supports1Gbps speed for full use of GMII interface data signals and also supports 10Mbps or 100Mbps for use of a subset of the GMII interface signals with configurable duplex operation [8, 9]. There are two GMII interface mode i.e.; internal GMII and external GMII mode. Internal GMII is used with integration of 1000BASE-X PCS/PMA core to provide fiber link and external GMII is used to connect with external PHY Chip to provide UTP link at speed of 1000Mbps. The MAC is independent and can be connected to any type of physical layer device. It also supports VLAN frames, inter-frame gap (IFG) and Frame Check Sequence (FCS). Figure 4 illustrates the remaining functional blocks of the core.

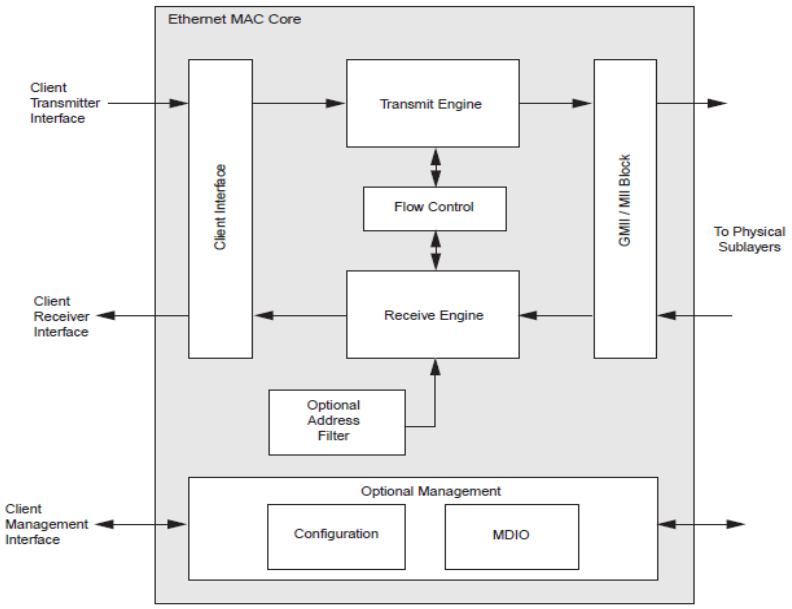

Figure 4. Block Diagram of Tri Mode Ethernet MAC core [6]

The transmit Engine accepts the Ethernet frame data from the Client Transmitter Interface, adds preamble field to the start of the frame, adds padding if required to meet the minimum frame length. It also adds FCS and ensures the minimum specified inter-frame gap between successive frames. The frames are then converted into the format that is compatible with GMII/MII and sent to the GMII/MII.

The Receive Engine accepts Ethernet frame data from the GMII Block and removes the preamble field at the start of the frame. It also removes padding bytes and Frame Check Sequence. The receiver also performs error detection on the received frame using information such as the frame check sequence field, received GMII error codes and legal frame size boundaries. The frames are then sent to the Client Receiver Interface. The Flow Control block is used to configure the MAC core that sends pause frames and act upon their reception during full-duplex operation.

The Address Filter checks the address of incoming frames into the receiver. If the Address Filter is enabled, the receiver does not pass the frame that contains one of a set of known addresses to the client. MDIO interface is used to access the configuration registers of the core and also used to access the configuration and status registers of a physical layer device (PHY). When the Management Interface is disabled, the core is configured via an alternative configuration vector. The gtx_clk 125MHz is used to implement GMII transmitter logic and GMII receiver logic for use at 1-Gbps.

2.3 Overall Design Architecture

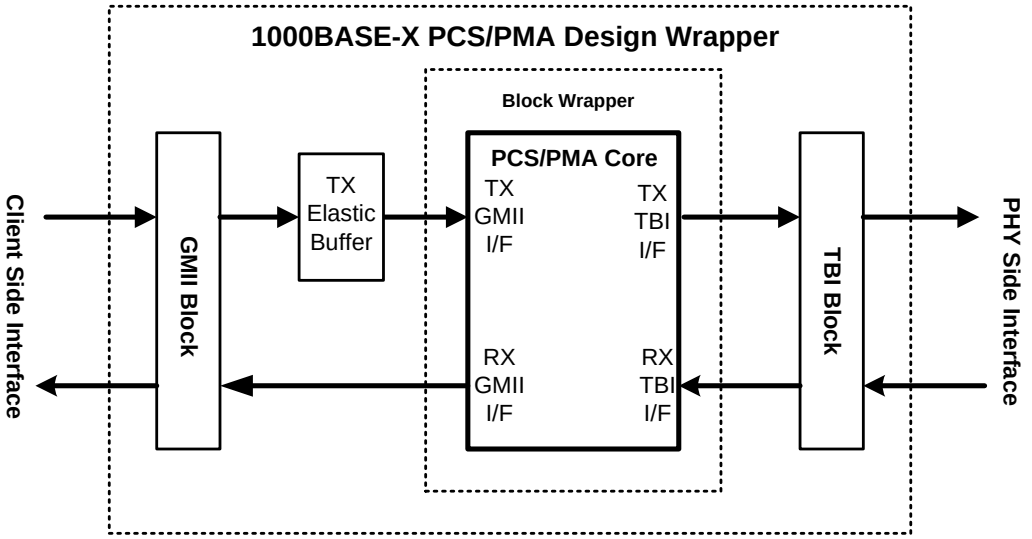

Figure 5. 1000BASE-X PCS/PMA core with Wrapper Design

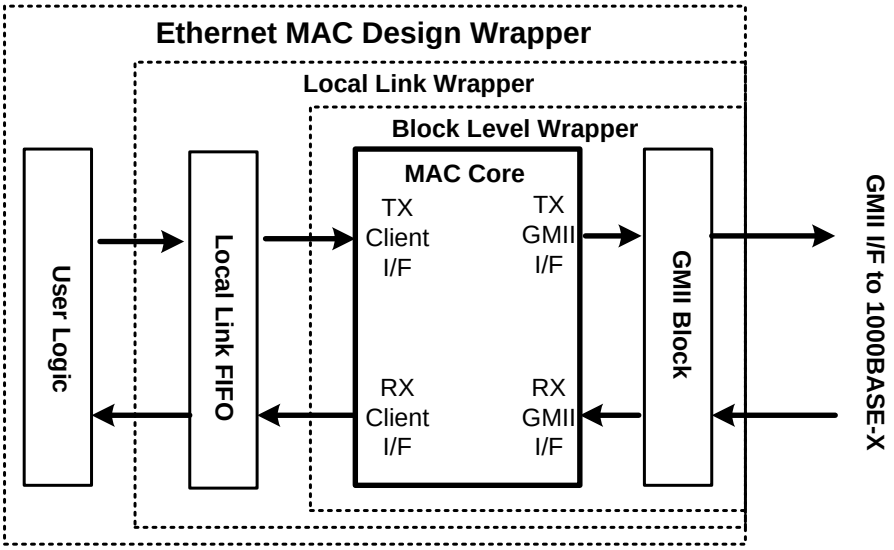

Figure 6. Ethernet MAC core with Wrapper Design

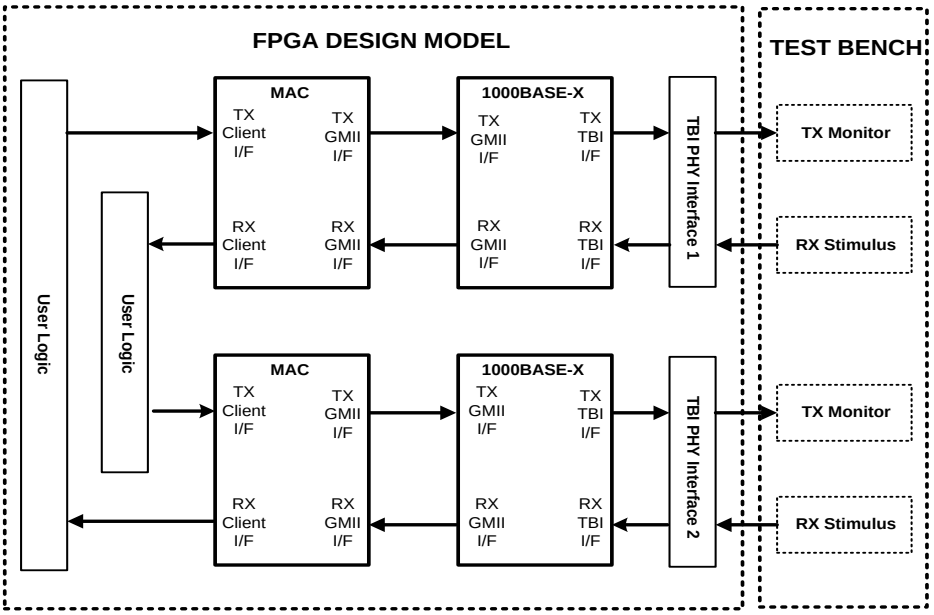

Figure 7. FPGA Design Model with Test Bench

2.3 Synthesized Results

In this paper, the synthesis part is performed on a customized Spartan 3E FPGA Board (xc3s500e-4fg320 package) using Xilinx ISE 14.7 Design Suite [10]. Furthermore, the verification of data integrity is carried out using Xilinx ISim simulator. The device utilization report of the proposed model is shown as in Figure 8.

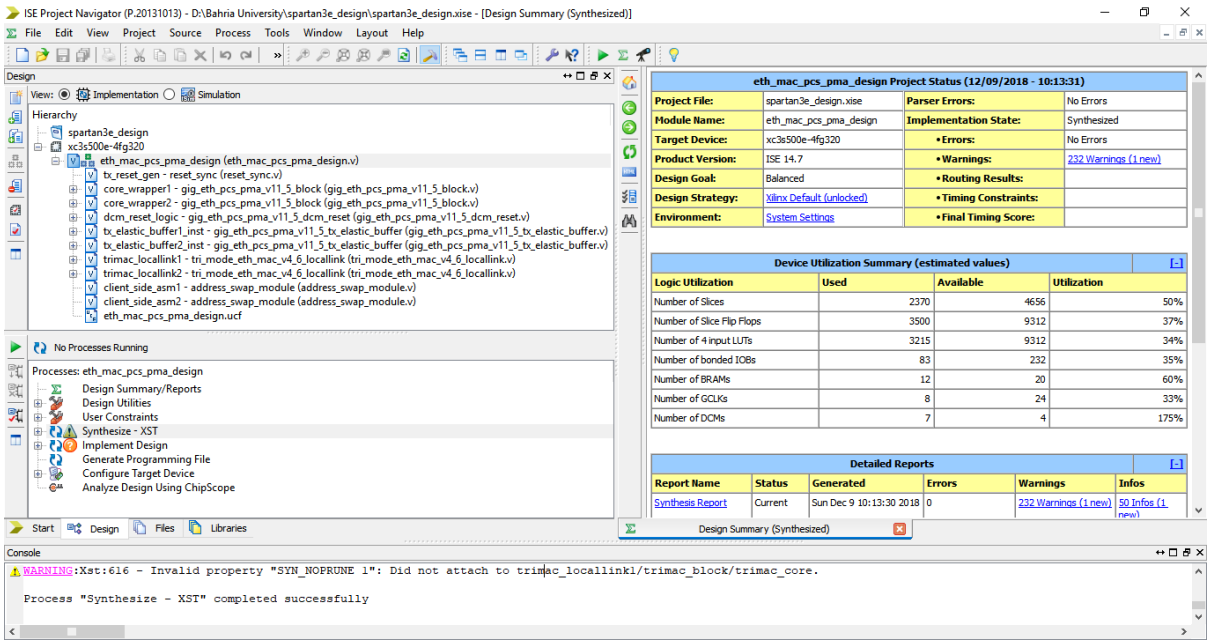

Figure 8. Schematic Diagram of Proposed Model

The RTL schematic for the proposed model is depicted in Figure 9. RTL schematic shows clearly input and output of each block and also interconnection between them.

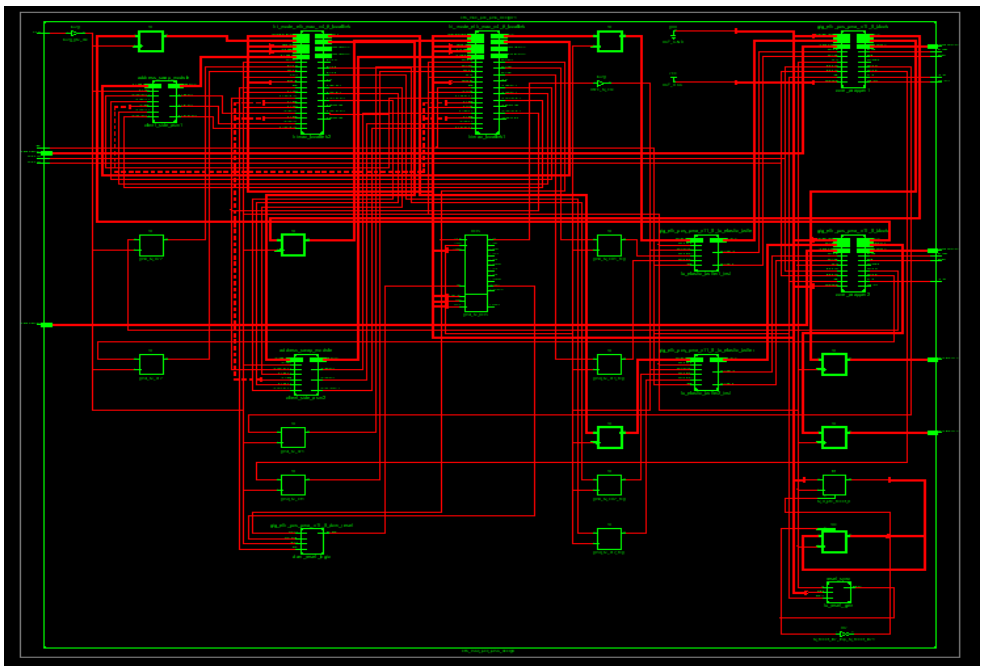

Figure 9. RTL Schematic Diagram of Proposed Model

3. Simulation Results

Many Simulators are used widely for debugging and testing of FPGAs design on the computer. The Xilinx ISE 14.7 ISim Simulator is used for testing and debugging of design. Simulation of the 1000BASE-X PCS/PMA and Tri-Mode Ethernet MAC core is tested by using the test bench. Moreover, sending and receiving frames separately are shown in Figure 10 and Figure 11. The frames are transmitted through the GMII transmitter interface and received through the GMII receiver interface

by PHY side interface loopback. The code was simulated of overall proposed design through sending the frames at TBI receiver interface and receiving the frames at TBI transmitter interface as shown in Figure 12.

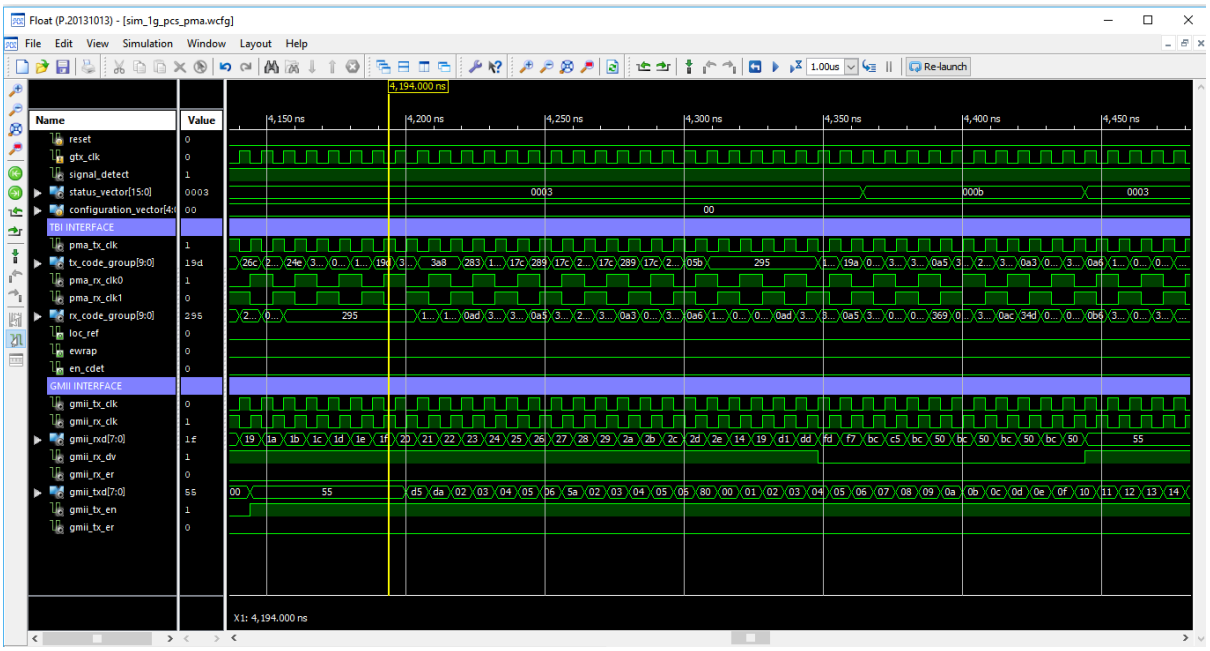

Figure 10. Simulation results of 1000BASE-X PCS/PMA with TBI core

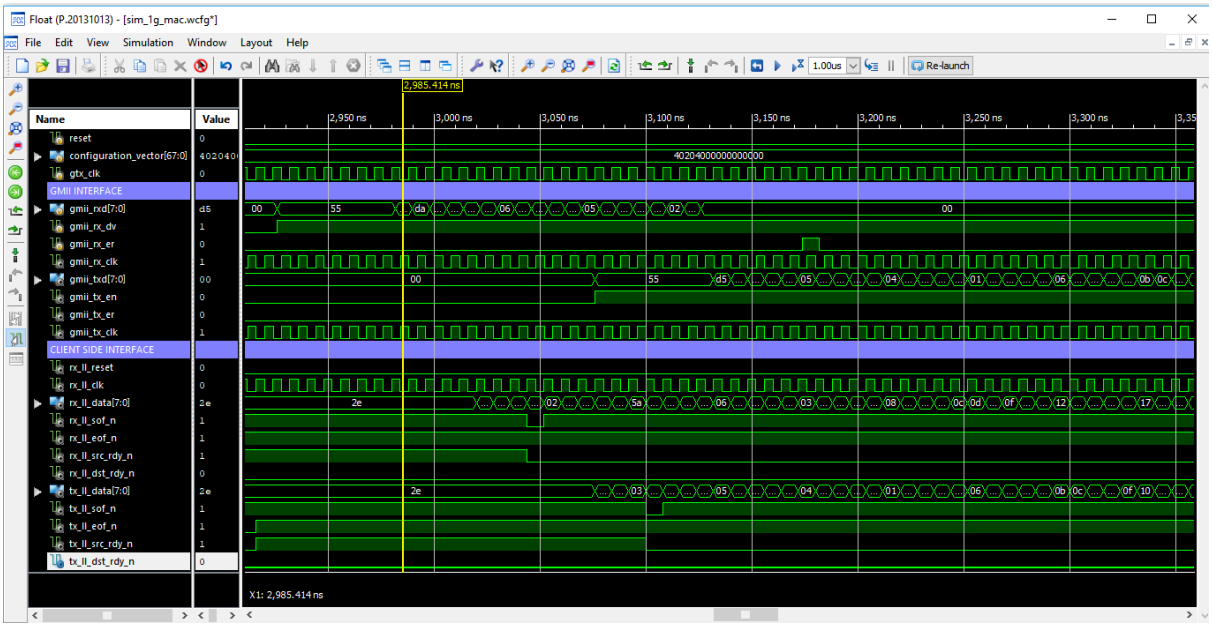

Figure 11. Simulation results of Tri Mode Ethernet MAC core

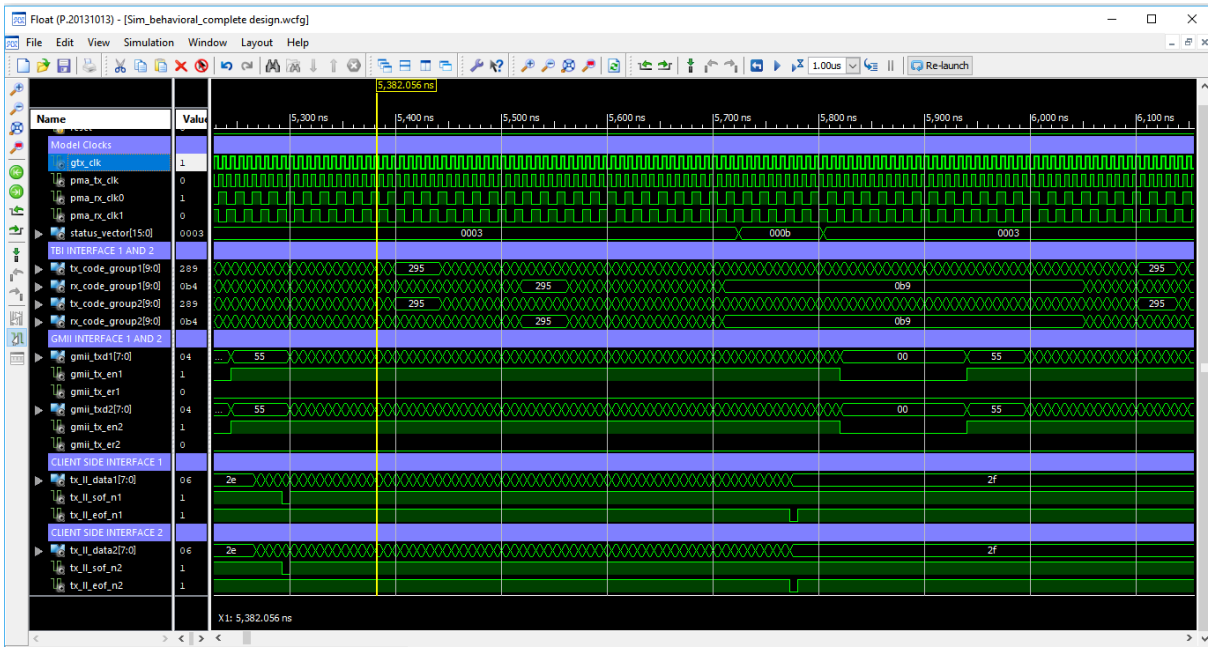

Figure 12. Simulation results of Proposed FPGA design

4. Conclusion

Day by day, the demand of high performance in terms of maximum bandwidth, low cost solution, high performance networks and data security. To provide the high-speed connectivity and data security, FPGA (Field Programmable Gate Array) based solution plays an important role over a large network. This paper introduces the implementation of both 1000BASE-X and Ethernet MAC Cores and provides the solution for communication link at high speed with low cost, low power consumption and high performance over fiber optics as well as a copper medium. The implementation of RTL (Register Transfer Level) model is achieved to develop and integrate the mentioned cores using Verilog HDL (Hardware Description Language). The Verilog HDL code is simulated for customized Xilinx Spartan 3E FPGA Board using Xilinx ISE 14.7 Design Suite. In future, this design may be used in string comparisons for Intrusion detection or in encryption/decryption for secure communication.

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